Floating Gat Transistors And Methods Of Forming Floating Gate Transistors

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor processing methods of forming floating gate transistors and to floating gate transistors.

BACKGROUND

[0002] Increased device performance is a continuing goal of efforts in advancing the semiconductor arts. For nonvolatile memory devices such as a programmable read only memory (PROM), increased device performance has been realized by improvements in both the programmability and erasure of the stored information. For example, early PROM devices were erased using exposure of the integrated circuit to ultra-violet light for a period of time on the order of twenty minutes to erase the entirety of the stored memory. Newer devices such as an electrically erasable programmable read only memory (EEPROM), as the name implies, are erasable using an electrical signal. While such EEPROM devices have reduced erasure time, the electrical signal employed for erasing is at a higher than normal voltage that results in a limiting of the number of times the device can be erased and reprogrammed. In addition, generally, erasing such EEPROM devices results in all stored information being erased.

[0003] More recently developed devices such as the flash-EEPROM device have provided the ability to used normal electrical voltages for erasure as well as providing for partial erasures. As such erasures and subsequent reprogramming are possible at essentially "normal" semiconductor speeds, flash-EEPROM devices are also generally referred to as a flash random access memory device or flash-RAM. With the increased performance of the flash-RAM, it has become desirable to increase the density of the memory storage units which generally encompass both a floating gate and a control gate for each unit. One problem with forming devices with such increased density has been the forming of the floating gate structures using generally known photolithographic methods. Therefore it would be desirable to provide alternative methods for forming floating gate transistor structures as well as the structures formed employing such methods.

SUMMARY

[0004] Exemplary embodiments of forming floating gate transistor structures in accordance with the present invention employ providing a substrate encompassing semiconductive material. A first layer is formed over the semiconductive material. At least one pair of spaced shallow trench isolation (STI) structures are formed extending through the first layer and into the semiconductive material, and at least a portion of the first layer between the spaced STI structures is removed effective to form a recess there between. The recess is at least partially filled by forming a conductive floating gate material therein and a control gate is formed operatively over the conductive floating gate material to form the floating gate transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings. For ease of understanding and simplicity, where the element is the same between drawings common numbering of elements within such drawings is employed.

[0006] Fig. 1 is a cross-sectional representation of a portion of a semiconductor substrate at an early process stage of an exemplary embodiment of the present invention.

[0007] Fig. 2 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 1 at a subsequent process stage of an exemplary embodiment of the present invention.

[0008] Fig. 3 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 2 at a subsequent process stage of an exemplary embodiment of the present invention.

[0009] Fig. 4 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 3 at a subsequent process stage of an exemplary embodiment of the present invention.

[0010] Fig. 5 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 4 at a subsequent process stage of an exemplary embodiment of the present invention.

[0011] Fig. 6 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 5 at a subsequent process stage of an exemplary embodiment of the present invention.

[0012] Fig. 7 is a cross-sectional representation of a portion of a semiconductor substrate of another exemplary embodiment of the present invention resulting from the substrate depicted in Fig. 5 and an alternate subsequent process stage

[0013] Fig. 8 is a cross-sectional representation of a portion of a semiconductor substrate of another exemplary embodiment of the present invention resulting from the substrate depicted in Fig. 4 and an alternate subsequent process stage.

[0014] Fig. 9 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 8 at a subsequent process stage of an exemplary embodiment of the present invention.

[0015] Fig. 10 is a cross-sectional representation of a portion of a semiconductor substrate of another exemplary embodiment of the present invention resulting from the substrate depicted in Fig. 5 and an alternate subsequent process stage.

[0016] Fig. 11 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 10 at a subsequent process stage of another exemplary embodiment of the present invention.

[0017] Fig. 12 is a cross-sectional representation of the portion of a semiconductor substrate depicted in Fig. 11 at a subsequent process stage of an exemplary embodiment of the present invention.